

FIG. 1

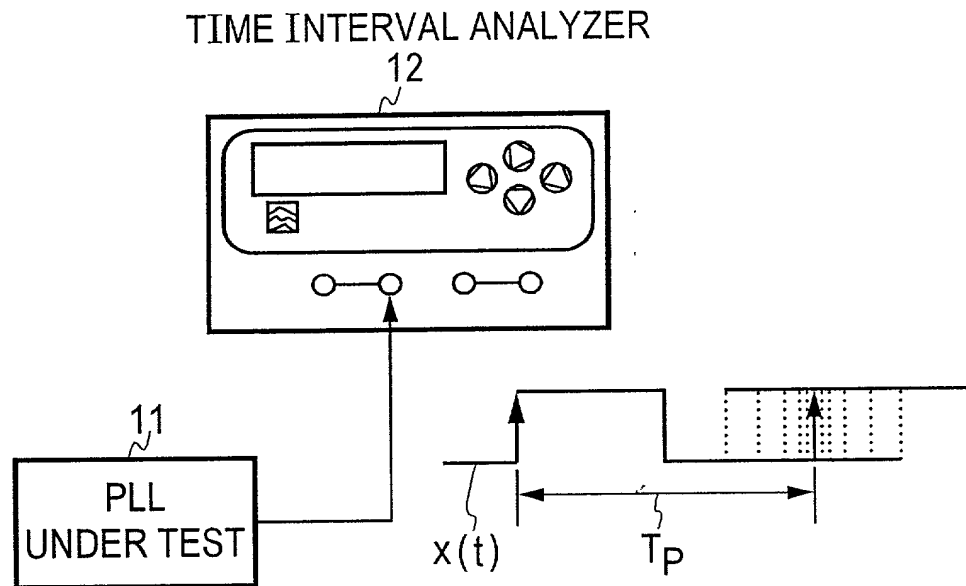


FIG. 2

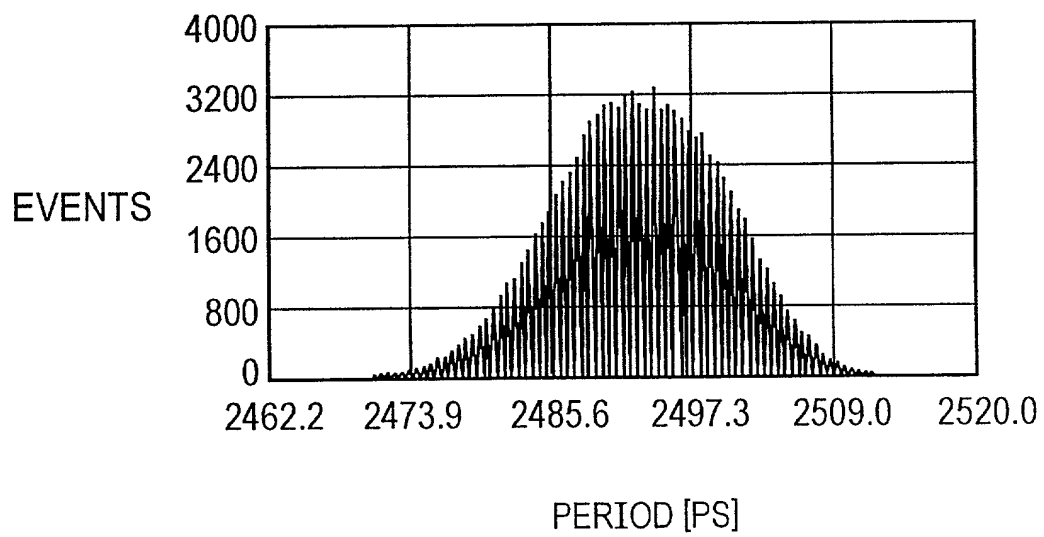


FIG. 3

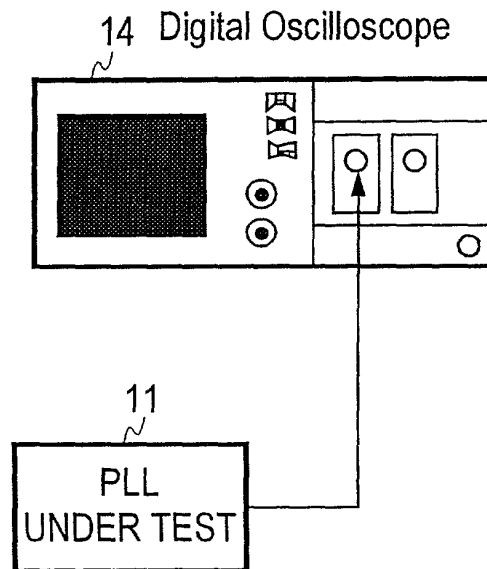


FIG. 4

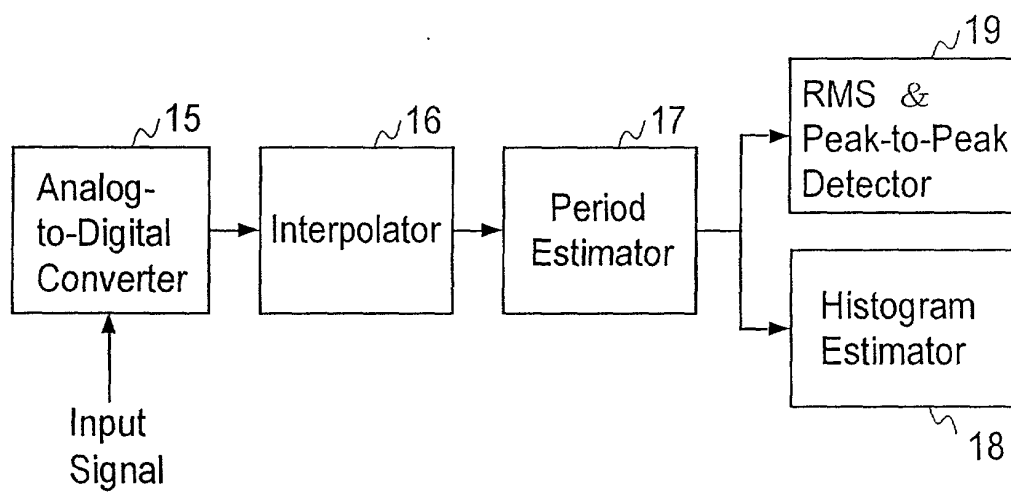


FIG. 5A

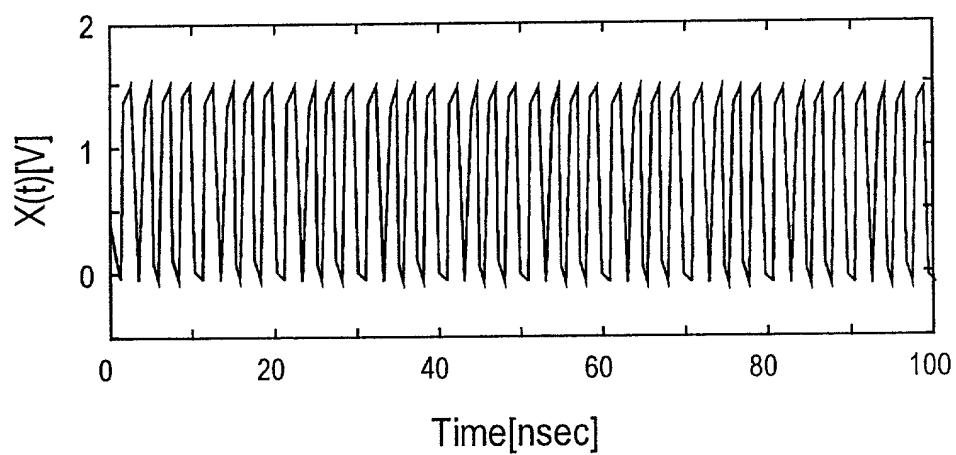
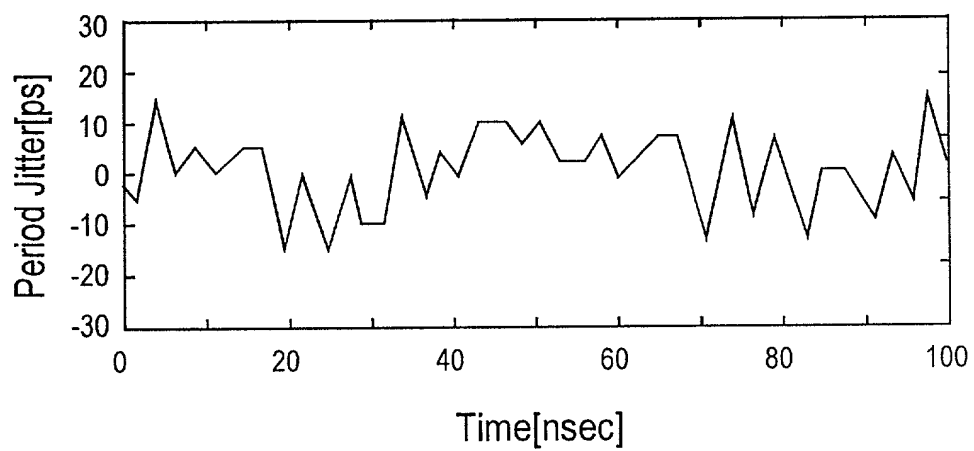


FIG. 5B



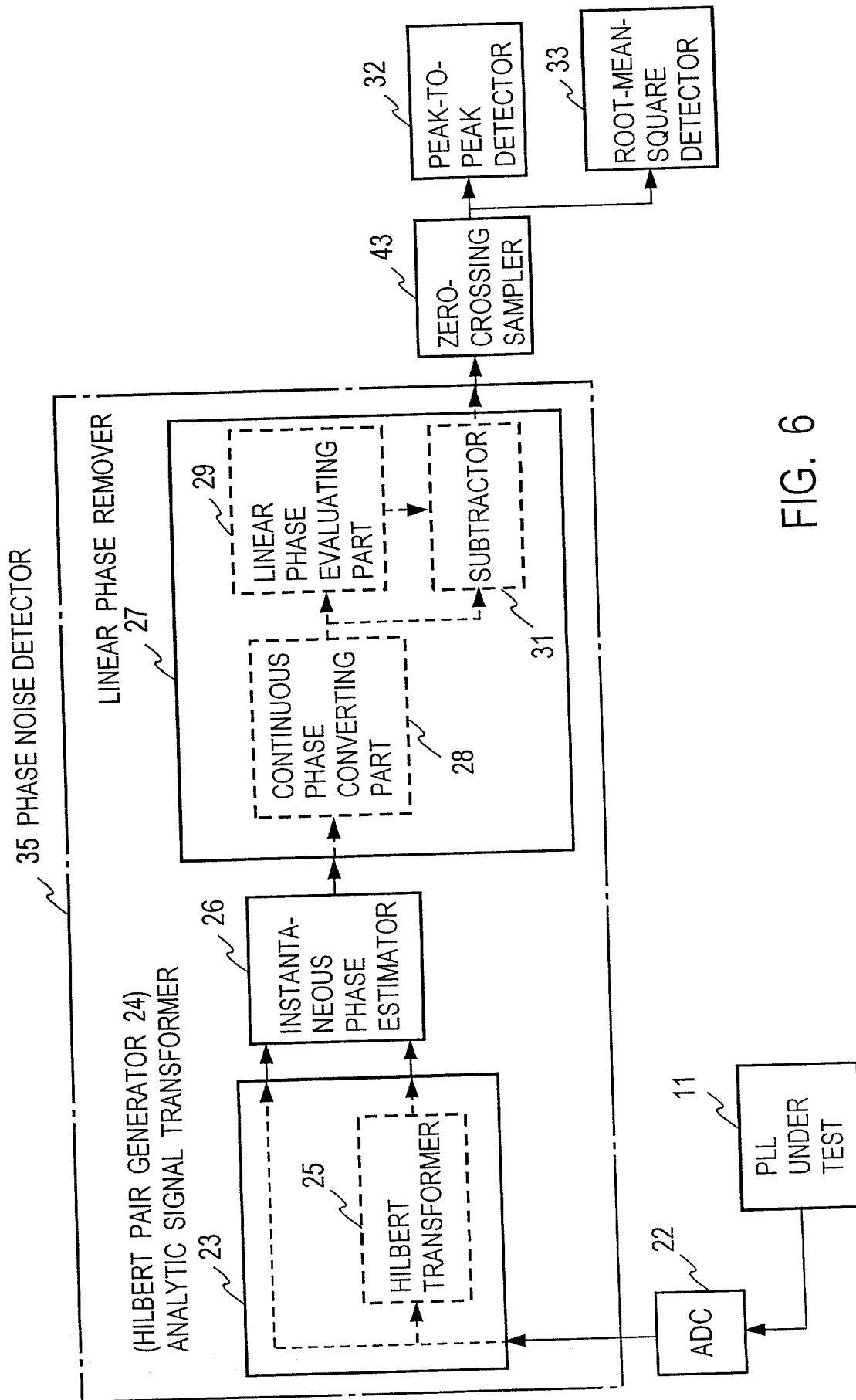


FIG. 6

FIG. 7

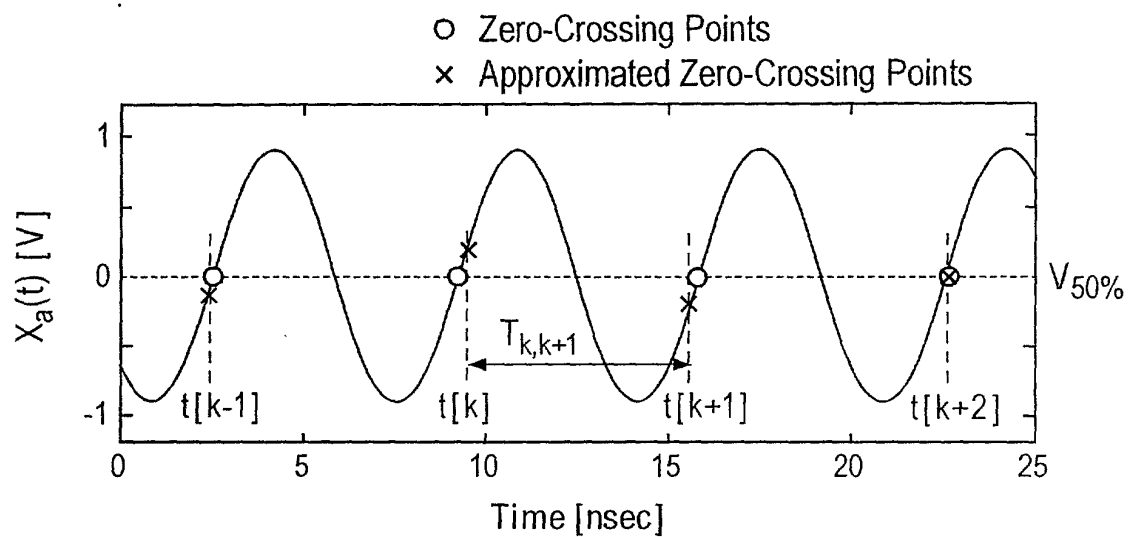


FIG. 8

Method	No. of Events	$J_{RMS}$	$J_{pp}$
$\Delta\phi$ Method	23,255	2.4534 ps (+0.5%)	8.0029 ps (+15.9%)
Corrected $\Delta\phi$ Method	23,255	2.4404 ps (-0.004%)	8.0029 ps (+0.04%)
Ideal Value	--	2.4405 ps	6.9028 ps

FIG. 9A

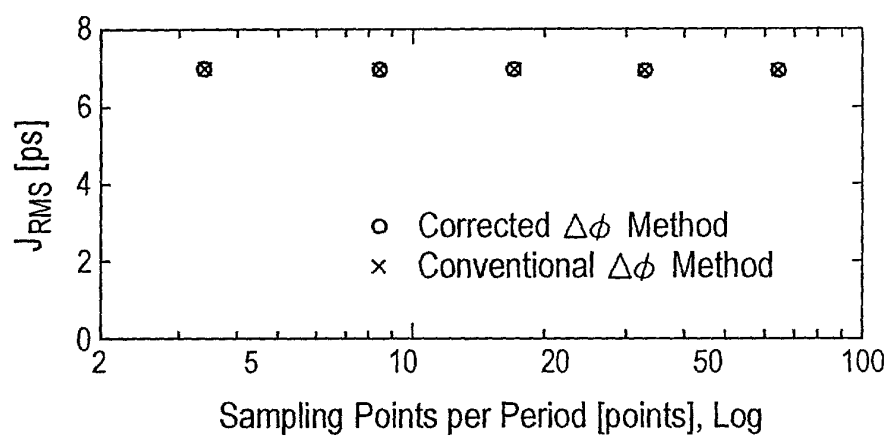


FIG. 9B

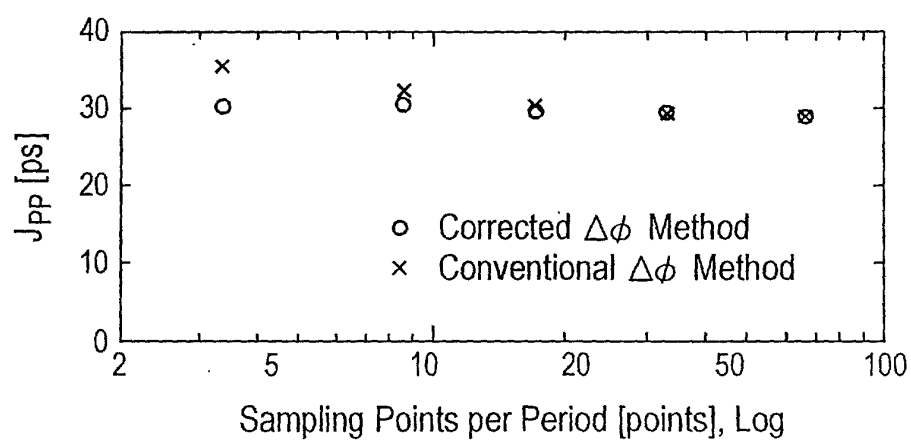


FIG. 10A

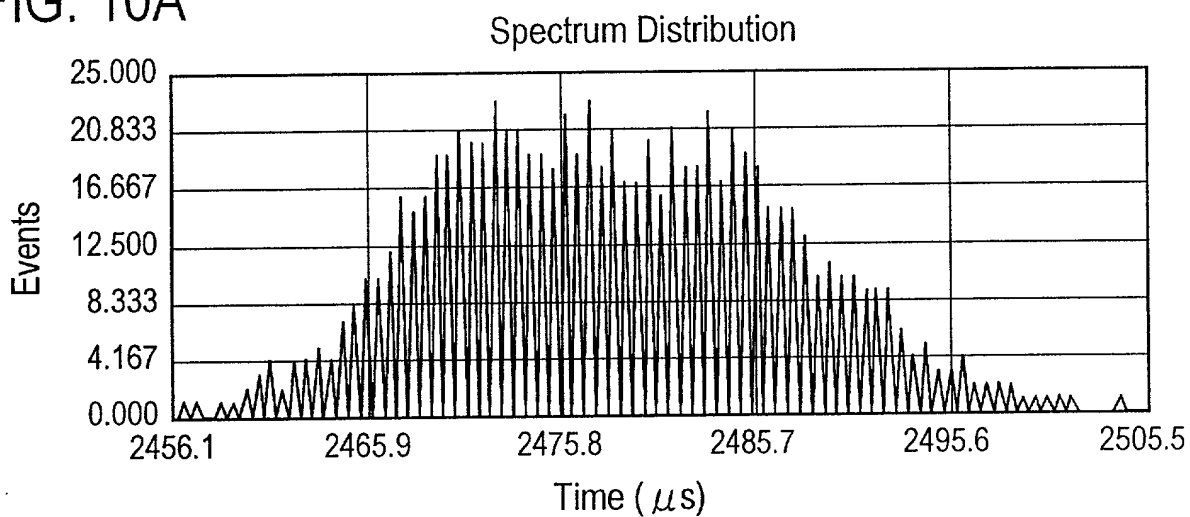


FIG. 10B

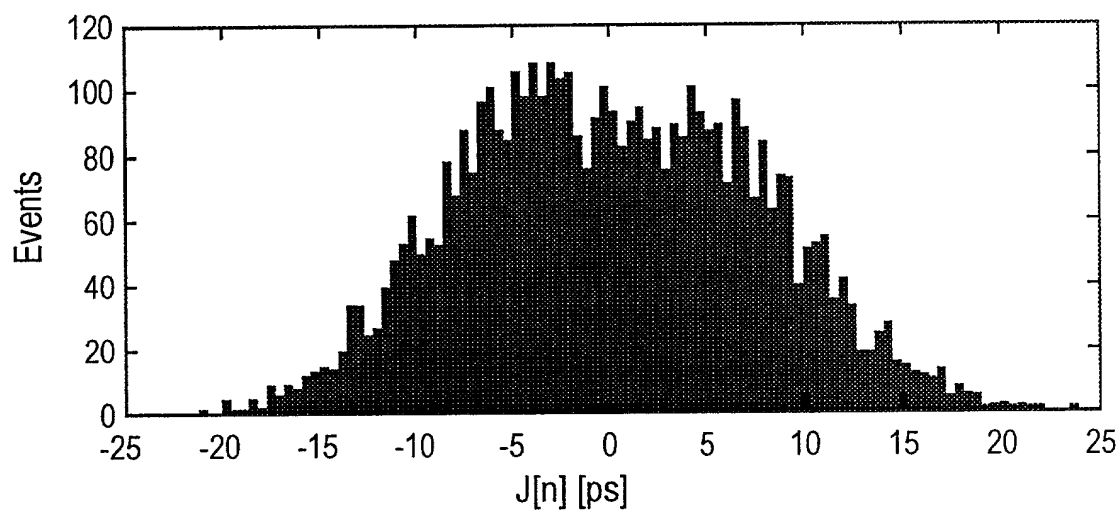


FIG. 11

Method	No. of Events	$J_{\text{RMS}}$	$J_{\text{pp}}$
Time Interval Analyzer	10,000	7.72 ps	48.2 ps
Corrected $\Delta\phi$ Method	4,696	7.48 ps	45.2 ps
Difference	-53%	-3.1%	+0.4%





FIG. 13 is a block diagram of a PLL under test system. The system includes a PLL under test (11) which outputs a signal to a divider (81) labeled 1/N. The output of the divider (81) is fed into an ADC (22). The output of the ADC (22) is fed into an analytic signal transformer (23). The analytic signal transformer (23) consists of three blocks: an FFT block (61), a BPF block (62), and an IFFT block (63). The output of the IFFT block (63) is the final output of the system.

FIG. 13

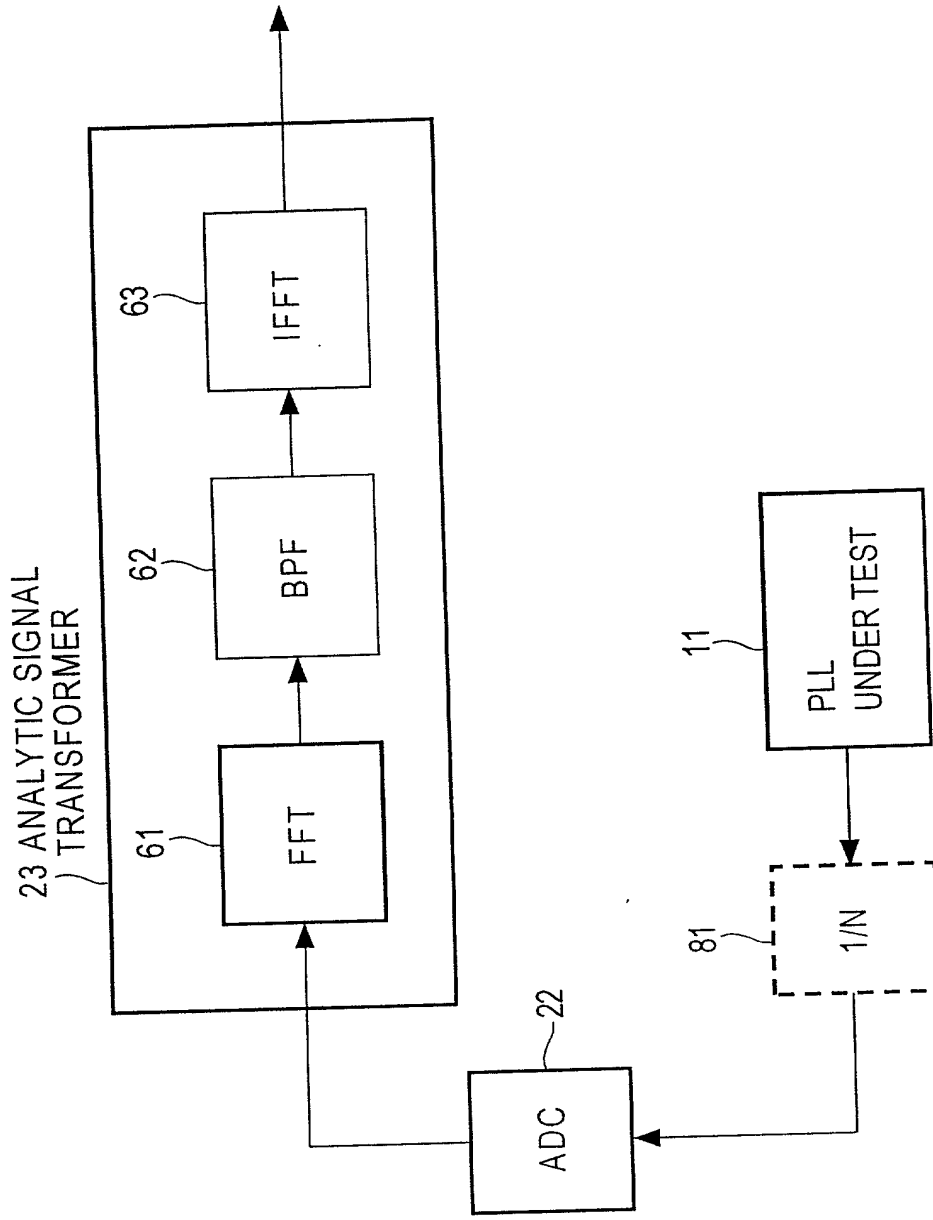


FIG. 14

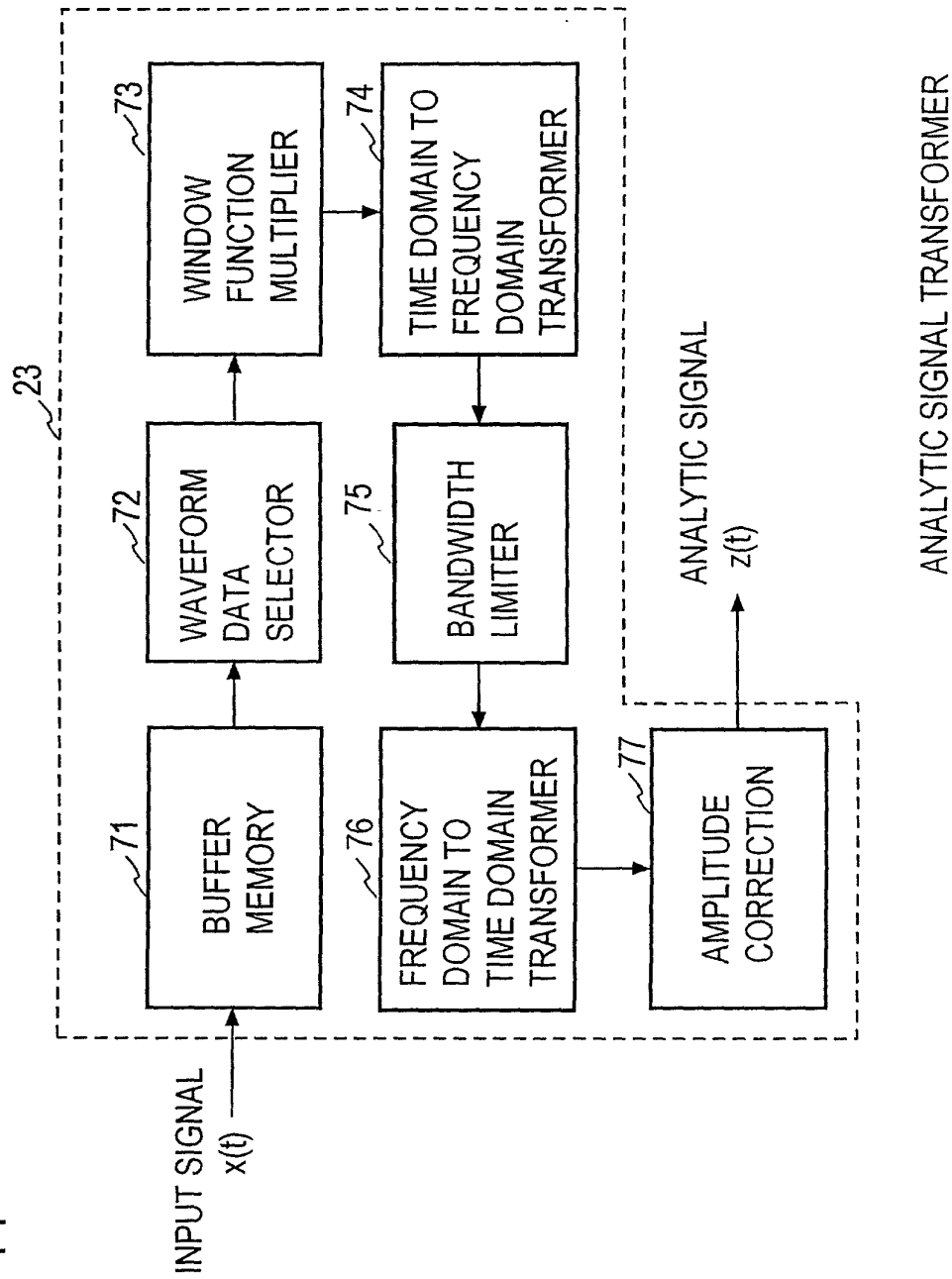
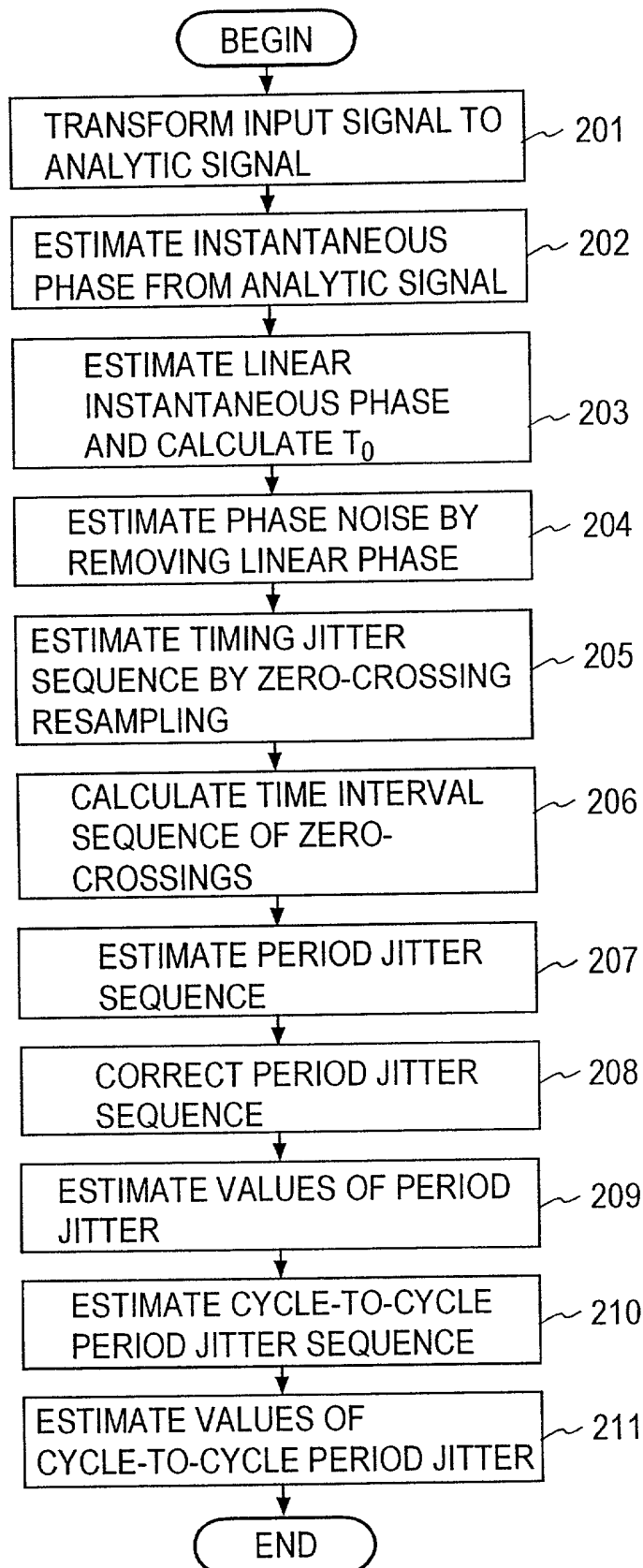


FIG. 15



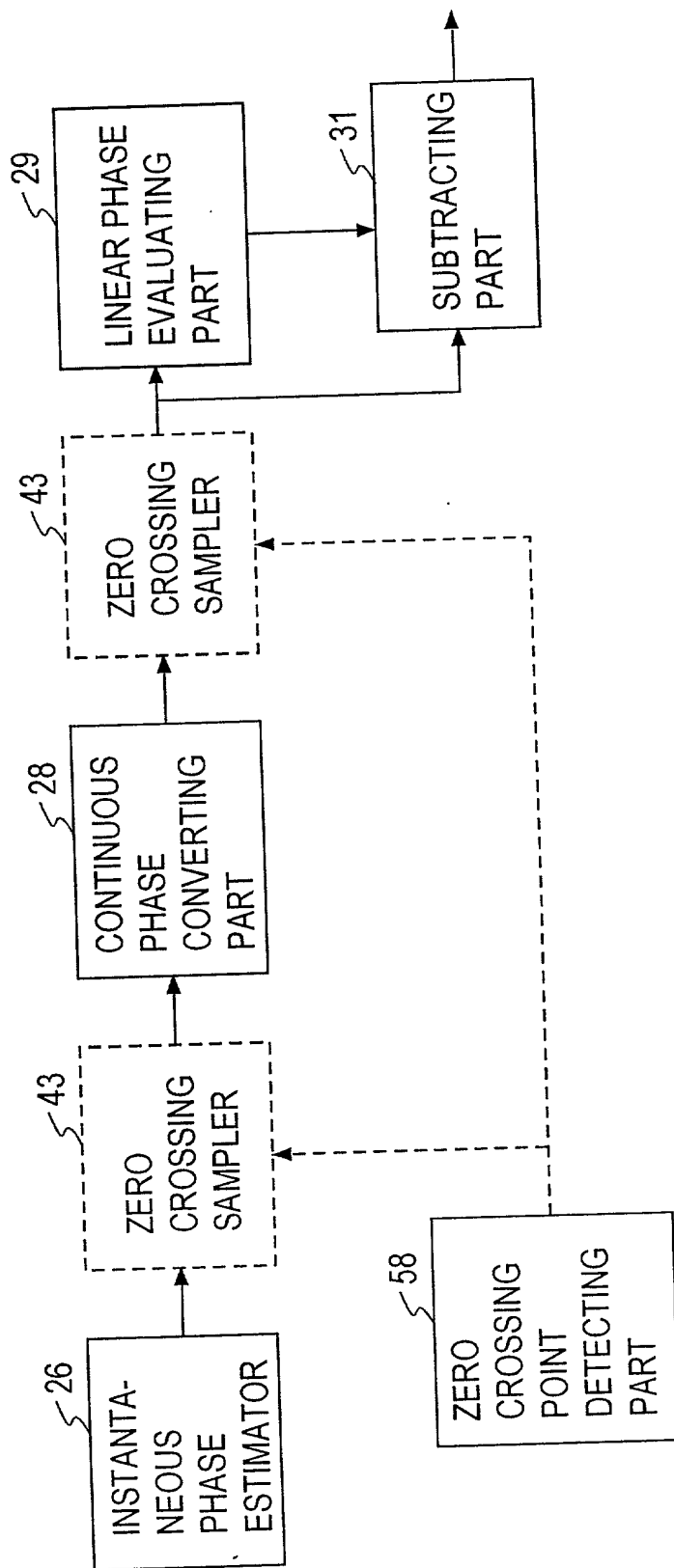


FIG. 16

FIG. 17

